USB 2.0 Hi-Speed Peripheral Compliance Test Report

USB-IF Compliance Program	
Company Name	SUPREMA INC.
Product Name	RealScan-G1
Model Number	RS-G1
Product Revision	V01B
Test Date	June 8, 2012
Test Result	**PASS**

TTA 한국정보통신기술협회 Telecommunications Technology Association
267-2, Seohyeon-dong, Bundang-gu, Seongnam-city, Gyeonggi-do, Korea.
Tel: +82-10-5111-1178, E-mail: jless@tta.or.kr, Fax: +82-31-724-0169.

A. Vendor and Product Information

Vendor Information
■ Vendor Name: SUPREMA INC. ■ Vendor Complete Address: 16F, Parkview Tower, Bundang-gu, Seongnam-City, Gyeonggi-Do KOREA ■ Vendor Phone Number: +82-31-710-2442 ■ Vendor Contact(s) – Name: Hyeonggak Lim Tel: +82-31-710-2442 E-mail: hglim@suprema.co.kr
Product Information
■ Silicon Model Name: Cypress, CY7C68013A ■ TID(if you know): 10006715 VID: 0x16d1 PID: 0x1027 ■ Product Category: Retail, Peripherals, High-Speed ■ Product Description: HS Peripheral/Others ☒ High Power ☐ Low Power ☒ Bus Powered ☐ Self Powered (Battery Powered) ☐ Untethered ☒ Tethered ■ Tested OS: ☒ Windows 7 ☐ Windows XP
Tested By Joonsi Jung

Overall Test Result: PASS

B. Legacy USB Compliance Tests

B.1 Frameworks Test Results: ☒ Pass ☐ Fail

Device Summary:

Interface: 1 MAX Power: 300 mA Self-powered: No Remote Wakeup: No

Comments:

Chapter 9:

High Speed Mode:	☒ Pass ☐ Fail
Full Speed Mode:	☒ Pass ☐ Fail
High Speed Mode on the SS Port:	☒ Pass ☐ Fail

B.2 Interoperability Test Overall Results: ☒ Pass ☐ Fail

EHCI Controller: (Intel DG965SS Motherboard)

1. Enumeration and Driver installation	☒ Pass	☐ Fail	
2. Operation with Default Driver	☒ Pass	☐ Fail	
3. Update Driver	☒ Pass	☐ Fail	☐ N/A
4. Install Additional Software	☒ Pass	☐ Fail	☐ N/A
5. DUT Demonstrates Operation	☒ Pass	☐ Fail	☐ N/A
6. DUT Operation Speed	☒ Pass	☐ Fail	
7. Interoperability – Operate all devices	☒ Pass	☐ Fail	
8. Hot Detach & Reattach	☒ Pass	☐ Fail	
9. Topology Change	☒ Pass	☐ Fail	
10. Warm Boot	☒ Pass	☐ Fail	
11. Cold Boot	☒ Pass	☐ Fail	
12. Remote Wake-up – Active S3 Suspend and Resume	☐ Pass	☐ Fail	☒ N/A
13. Active S3 Suspend and Resume	☒ Pass	☐ Fail	
14. Active S4 Hibernate and Resume	☒ Pass	☐ Fail	

UHCI Controller: (Intel DG965SS Motherboard)

1. Enumeration	☒ Pass	☐ Fail
2. Interoperability – Operate all devices	☒ Pass	☐ Fail
3. Suspend and Resume	☒ Pass	☐ Fail
4. Warm Boot	☒ Pass	☐ Fail

OHCI Controller: (NEC AUA4000 PCI Adapter)

1. Enumeration	☒ Pass	☐ Fail
2. Interoperability – Operate all devices	☒ Pass	☐ Fail
3. Suspend and Resume	☒ Pass	☐ Fail
4. Warm Boot	☒ Pass	☐ Fail

B.3 Current Measurement Results: ☒ **Pass** ☐ Fail

High Speed Mode: ☒ Pass ☐ Fail

Operating current: 221 mA

Unconfigured current: 37 mA

Configured current: 133 mA

Suspend current: 0.5 mA

Powered Stated Suspend Current**:** 0.5 mA

Full Speed Mode: ☒ Pass ☐ Fail

Operating current: 141 mA

Unconfigured current: 24 mA

Configured current: 118 mA

Suspend current: 0.4 mA

Powered Stated Suspend Current**:** 0.4 mA

B.4 Full-speed Upstream Signal Quality Test Result: ☒ **Pass** ☐ Fail

B.5 Inrush Current Test: ☒ **Pass** ☐ Fail

B.6 Back Voltage Test Results: (Enumerate before/after) ☒ **Pass** ☐ Fail

D+: 0 mV / 0 mV

D- : 0 mV / 0 mV

V_{Bus}: 0 mV / 0 mV

(All values <= 400mV)

B7 Enumeration Test on USB3.0 Port: ☒ **Pass** ☐ Fail

C. Device High-Speed Electrical Tests

C.1 Device High-speed Signal Quality (EL_2, EL_4, EL_5, EL_6, EL_7)

EL_2 A USB 2.0 high-speed transmitter data rate must be 480 Mb/s ± 0.05%.

Reference documents: *USB 2.0 Specification*, Section 7.1.11

☒ **Pass** ☐ Fail ☐ N/A

Comments:

EL_4 A USB 2.0 upstream facing port on a device without a captive cable must meet Template 1 transform waveform requirements measured at TP3.

Reference documents: *USB 2.0 Specification*, Section 7.1.2.2

☐ Pass ☐ Fail ☒ N/A

Comments:

EL_5 A USB 2.0 upstream facing port on a device with a captive cable must meet Template 2 transform waveform requirements measured at TP2.

Reference documents: *USB 2.0 Specification*, Section 7.1.2.2

☒ **Pass** ☐ Fail ☐ N/A

Comments:

EL_6 A USB 2.0 HS driver must have 10% to 90% differential rise and fall times of greater than 500ps.

Reference documents: *USB 2.0 Specification*, Section 7.1.2.2

☒ **Pass** ☐ Fail ☐ N/A

Comments:

EL_7 A USB 2.0 HS driver must have monotonic data transitions over the vertical openings specified in the appropriate eye pattern template.

Reference documents: *USB 2.0 Specification*, Section 7.1.2.2

☒ **Pass** ☐ Fail ☐ N/A

Comments:

C.2 Device Packet Parameters (EL_21, EL_22, EL_25)

EL_21 The SYNC filed for all transmitted packets (not repeated packets) must begin with a 32-bit SYNC field.

Reference documents: *USB 2.0 Specification*, Section 8.2

Result: 64.613 ns

☒ **Pass** ☐ Fail ☐ N/A

Comments:

EL_22 When transmitting after receiving a packet, hosts and devices must provide an inter-packet gap of a t least 8 bit times and not more than 192 bit times.

Reference documents: *USB 2.0 Specification*, Section 7.1.18.2

Result: 299.728, 251.608 ns

☒ **Pass** ☐ Fail ☐ N/A

Comments:

EL_25 The EOP for all transmitted packets (except SOFs) must be an 8-bit NRZ byte of 01111111 without bit stuffing. *(**Note**, that a longer EOP is waiverable)*

Reference documents: *USB 2.0 Specification*, Section 7.1.13.2

Result: 17.139 ns

☒ **Pass** ☐ Fail ☐ N/A

Comments:

C.3 Device CHIRP Timing (EL_28, EL_29, EL_31)

EL_28 Devices must transmit a chirp handshake no sooner than 2.5us and no later than 3ms when being reset from suspend or a full-speed state.

Reference documents: *USB 2.0 Specification*, Section 7.1.7.5

Result: 2.065307 ms

☒ **Pass** ☐ Fail ☐ N/A

Comments:

EL_29 The chirp handshake generated by a device must be at least 1ms and not more than 7ms in duration.

Reference documents: *USB 2.0 Specification*, Section 7.1.7.5

Result: 2.003 ms

☒ **Pass** ☐ Fail ☐ N/A

Comments:

EL_31 During device speed detection, when a device detects a valid Chirp K-J-K-J-K-J sequence, the device must disconnect its 1.5K pull-up resistor and enable its high-speed terminations within 500us.

Reference documents: *USB 2.0 Specification*, Section 7.1.7.5

Result: 4.182 us

☒ **Pass** ☐ Fail ☐ N/A

Comments:

C.4 Device Suspend/Resume/Reset Timing (EL_27, EL_28, EL_38, EL_39, EL_40)

EL_38 A device must revert to full-speed termination no later than 125us after there is a 3ms idle period.

Reference documents: *USB 2.0 Specification*, Section 7.1.7.6

Result: 3.004 ms

☒ **Pass** ☐ Fail ☐ N/A

Comments:

EL_39 A device must support the Suspend state.

Reference documents: *USB 2.0 Specification*, Section 7.1.7.6

☒ **Pass** ☐ Fail ☐ N/A

Comments:

EL_40 If a device is in the suspend state, and was operating in high-speed before being suspended, then device must transition back to high-speed operation within two bit times from the end of resume signaling.

*(**Note**. It is not feasible to measure the device transition back to high-speed operation within two bit times from the end of the resume signaling. The presence of SOFs at nominal 400mV amplitude following the resume signaling is sufficient for this test)*

Reference documents: *USB 2.0 Specification*, Section 7.1.7.7

☒ **Pass** ☐ Fail ☐ N/A

Comments:

EL_27 Devices must transmit a chirp handshake no sooner than 3.1ms and no later than 6ms when being reset from a non-suspended high-speed mode. The timing is measured from the beginning of the last SOF transmitted before the reset begins.

Reference documents: *USB 2.0 Specification*, Section 7.1.7.5

Result: 4.506 ms

☒ **Pass** ☐ Fail ☐ N/A

Comments:

EL_28 A device must transmit a chirp handshake no sooner than 2.5us and no later than 3ms when being reset from suspend or a full-speed state.

Reference documents: *USB 2.0 Specification*, Section 7.1.7.5

Result: 2.067114 ms

☒ **Pass** ☐ Fail ☐ N/A

Comments:

C.5 Device Test J/K, SE0_NAK (EL_8, EL_9)

EL_8 When either D+ or D- are driven high, the output voltage must be 400mV ± 10% when terminated with precision 45 Ohm resistors to ground.

Reference documents: *USB 2.0 Specification*, Section 7.1.1.3

Test	D+ Voltage	D- Voltage
J	-	8 mV
K	9 mV	-

☒ **Pass** ☐ Fail ☐ N/A

Comments:

EL_9 When either D+ or D- are not being driven, the output voltage must be 0V ± 10mV when terminated with precision 45 Ohm resistors to ground.

Reference documents: *USB 2.0 Specification*, Section 7.1.1.3

	Voltage
D+	9 mV
D-	9 mV

☒ **Pass** ☐ Fail ☐ N/A

Comments:

C.6 Device Receiver Sensitivity (EL_16, EL_17, EL_18)

EL_18 A high-speed capable device's Transmission Envelope Detector must be fast enough to allow the HS receiver to detect data transmission, achieve DLL lock, and detect the end of the SYNC field within 12 bit times.

Reference documents: *USB 2.0 Specification*, Section 7.1

☒ **Pass** ☐ Fail ☐ N/A

Comments:

EL_17 A high-speed capable device must implement a transmission envelope detector that does not indicate squelch (i.e. reliably receive packets) when a receiver exceeds 150mV differential amplitude.

*(**Note**. A waiver may be granted if the receiver does not indicate Squelch at +/-50mV of 150mV differential amplitude. This is to compensate for the oscilloscope probe point away from the receiver pin)*

Reference documents: *USB 2.0 Specification*, Section 7.1

Results: 188.060 mV

☒ **Pass** ☐ Fail ☐ N/A

Comments: WAIVER

EL_16 A high-speed capable device must implement a transmission envelope detector that indicate squelch (i.e. never receive packets) when a receiver's input falls below 100mV differential amplitude.

*(**Note**. A waiver may be granted if the receiver indicates Squelch at +/-50mV of 100mV differential amplitude. This is to compensate for the oscilloscope probe point away from the receiver pin)*

Reference documents: *USB 2.0 Specification*, Section 7.1

Results: 170.340 mV

☒ **Pass** ☐ Fail ☐ N/A

Comments:

- The end of document-