



USB 2.0 Hi-Speed Peripheral Compliance Test Report

USB-IF Compliance Program	
Company Name	Suprema HQ Inc,
Product Name	BioMini Plus 2
Model Number	SFU550
Product Revision	V01A
Test Date	September 23, 2016
Test Result	PASS

Vendor Information	
■ Vendor Name:	<u>Suprema HQ Inc.</u>
■ Vendor Complete Address:	<u>16F Parkview Office Tower, 248, Jeongjail-ro, Bundang-gu, Seongnam-si, Gyeonggi-do, Korea</u>
■ Vendor Phone Number:	<u>+82-31-710-4741</u>
■ Vendor Contact(s) – Name:	<u>SuYeol Park</u>
	Tel: <u>+82-10-7195-0605</u>
	E-mail: <u>sypark2@suprema.co.kr</u>
Product Information	
■ Silicon Model Name:	<u>Cypress Semiconductor, EZ-USB FX2LP CY7C68013A(40460272)</u>
■ TID(if you know):	<u>10007587</u> VID: <u>0x16D1</u> PID: <u>0x0409</u>
■ Product Category:	<u>Retail/Peripherals/Hi-Speed</u>
■ Product Description:	<u>Live Fingerprint</u>
	<input checked="" type="checkbox"/> High Power <input type="checkbox"/> Low Power <input checked="" type="checkbox"/> Bus Powered <input type="checkbox"/> Self Powered <input type="checkbox"/> Battery Powered <input type="checkbox"/> Untethered <input checked="" type="checkbox"/> Tethered
■ Tested OS:	<input checked="" type="checkbox"/> Windows 10 <input type="checkbox"/> Windows 8 <input type="checkbox"/> Windows 7

TTA 한국정보통신기술협회
Telecommunications Technology Association

B. Legacy USB Compliance Tests

B.1 Frameworks Test Results:

☒ **Pass** ☐ Fail

Device Summary:

Interface: 1 MAX Power: 100 mA Self-powered: No Remote Wakeup: No
Comments:

Chapter 9:

High Speed Mode: ☒ Pass ☐ Fail

Full Speed Mode: ☒ Pass ☐ Fail

High Speed Mode on the SS Port: ☒ Pass ☐ Fail

B.2 Interoperability Test Overall Results:

☒ **Pass** ☐ Fail

Comments:

EHCI Controller: (StarTech.com PEX400USB2 PCI Express USB2.0 Adapter Card)

- | | |
|---------------------------------|--|
| 1. Driver installation | <input checked="" type="checkbox"/> Pass <input type="checkbox"/> Fail |
| 2. Enumeration | <input checked="" type="checkbox"/> Pass <input type="checkbox"/> Fail |
| 3. Interoperability | <input checked="" type="checkbox"/> Pass <input type="checkbox"/> Fail |
| 4. Active S3 Suspend and Resume | <input checked="" type="checkbox"/> Pass <input type="checkbox"/> Fail |
| 5. Boots | <input checked="" type="checkbox"/> Pass <input type="checkbox"/> Fail |

xHCI Controller: (DELL XPS8700 Host PC)

- | | |
|---|--|
| 1. Driver installation | <input checked="" type="checkbox"/> Pass <input type="checkbox"/> Fail |
| 2. Enumeration | <input checked="" type="checkbox"/> Pass <input type="checkbox"/> Fail |
| 3. Stress | <input checked="" type="checkbox"/> Pass <input type="checkbox"/> Fail |
| 4. Active S3 Suspend and Resume | <input checked="" type="checkbox"/> Pass <input type="checkbox"/> Fail |
| 5. Interoperability with USB3.1 Gold Tree | <input checked="" type="checkbox"/> Pass <input type="checkbox"/> Fail |

B.3 Current Measurement Results:

☒ **Pass** ☐ Fail

High Speed Mode:

☒ Pass ☐ Fail

Operating current: 48 mA

Unconfigured current: 48 mA

Configured current: 49 mA

Suspend current: 0 mA

Powered Stated Suspend Current: 0 mA

Full Speed Mode:

☒ Pass ☐ Fail

Operating current: 44 mA

Unconfigured current: 44 mA

Configured current: 44 mA

Suspend current: 0 mA

Powered Stated Suspend Current: 0 mA

B.4 Full-speed Upstream Signal Integrity Test Results:

☒ **Pass** ☐ Fail

Signal Quality Test

☒ Pass ☐ Fail

Rise Time Test

☒ Pass ☐ Fail

Fall Time Test

☒ Pass ☐ Fail**B.5 Inrush Current Test:**☒ **Pass** ☐ Fail**B.6 Back Voltage Test Results: (Enumerate before/after)**☒ **Pass** ☐ FailD+: 0 mV / 0 mVD- : 0 mV / 0 mVV_{Bus}: 0 mV / 0 mV

(All values <= 400mV)



C. Device High-Speed Electrical Tests

C.1 Device High-speed Signal Quality (EL_2, EL_4, EL_5, EL_6, EL_7)

EL_2 A USB 2.0 high-speed transmitter data rate must be 480 Mb/s \pm 0.05%.

Reference documents: *USB 2.0 Specification*, Section 7.1.11

☒ Pass ☐ Fail ☐ N/A

Comments:

EL_4 A USB 2.0 upstream facing port on a device without a captive cable must meet Template 1 transform waveform requirements measured at TP3.

Reference documents: *USB 2.0 Specification*, Section 7.1.2.2

☐ Pass ☐ Fail ☒ N/A

Comments:

EL_5 A USB 2.0 upstream facing port on a device with a captive cable must meet Template 2 transform waveform requirements measured at TP2.

Reference documents: *USB 2.0 Specification*, Section 7.1.2.2

☒ Pass ☐ Fail ☐ N/A

Comments:

EL_6 A USB 2.0 HS driver must have 10% to 90% differential rise and fall times of greater than 500ps.

Reference documents: *USB 2.0 Specification*, Section 7.1.2.2

☒ Pass ☐ Fail ☐ N/A

Comments:

EL_7 A USB 2.0 HS driver must have monotonic data transitions over the vertical openings specified in the appropriate eye pattern template.

Reference documents: *USB 2.0 Specification*, Section 7.1.2.2

☒ Pass ☐ Fail ☐ N/A

Comments:

C.2 Device Packet Parameters (EL_21, EL_22, EL_25)

EL_21 The SYNC field for all transmitted packets (not repeated packets) must begin with a 32-bit SYNC field.

Reference documents: *USB 2.0 Specification*, Section 8.2

Result: 64.600 ns

☒ Pass ☐ Fail ☐ N/A

Comments:

EL_22 When transmitting after receiving a packet, hosts and devices must provide an inter-packet gap of at least 8 bit times and not more than 192 bit times.

Reference documents: *USB 2.0 Specification*, Section 7.1.18.2

Result: 310.708, 263.917 ns

☒ Pass ☐ Fail ☐ N/A

Comments:

EL_25 The EOP for all transmitted packets (except SOFs) must be an 8-bit NRZ byte of 01111111 without bit stuffing. (*Note, that a longer EOP is waiverable*)

Reference documents: *USB 2.0 Specification*, Section 7.1.13.2

Result: 16.919 ns

☒ Pass ☐ Fail ☐ N/A

Comments:

C.3 Device CHIRP Timing (EL_28, EL_29, EL_31)

EL_28 Devices must transmit a chirp handshake no sooner than 2.5us and no later than 3ms when being reset from suspend or a full-speed state.

Reference documents: *USB 2.0 Specification*, Section 7.1.7.5

Result: 2.135926 ms

☒ Pass ☐ Fail ☐ N/A

Comments:

EL_29 The chirp handshake generated by a device must be at least 1ms and not more than 7ms in duration.

Reference documents: *USB 2.0 Specification*, Section 7.1.7.5

Result: 2.003 ms

☒ Pass ☐ Fail ☐ N/A

Comments:

EL_31 During device speed detection, when a device detects a valid Chirp K-J-K-J-K-J sequence, the device must disconnect its 1.5K pull-up resistor and enable its high-speed terminations within 500us.

Reference documents: *USB 2.0 Specification*, Section 7.1.7.5

Result: 4.180 us

☒ Pass ☐ Fail ☐ N/A

Comments:

C.4 Device Suspend/Resume/Reset Timing (EL_27, EL_28, EL_38, EL_39, EL_40)

EL_38 A device must revert to full-speed termination no later than 125us after there is a 3ms idle period.

Reference documents: *USB 2.0 Specification*, Section 7.1.7.6

Result: 3.005 ms

☒ Pass ☐ Fail ☐ N/A

Comments:

EL_39 A device must support the Suspend state.

Reference documents: *USB 2.0 Specification*, Section 7.1.7.6

☒ Pass ☐ Fail ☐ N/A

Comments:

EL_40 If a device is in the suspend state, and was operating in high-speed before being suspended, then device must transition back to high-speed operation within two bit times from the end of resume signaling.

(**Note.** It is not feasible to measure the device transition back to high-speed operation within two bit times from the end of the resume signaling. The presence of SOFs at nominal 400mV amplitude following the resume signaling is sufficient for this test)

Reference documents: *USB 2.0 Specification*, Section 7.1.7.7

☒ Pass ☐ Fail ☐ N/A

Comments:

EL_27 Devices must transmit a chirp handshake no sooner than 3.1ms and no later than 6ms when being reset from a non-suspended high-speed mode. The timing is measured from the beginning of the last SOF transmitted before the reset begins.

Reference documents: *USB 2.0 Specification*, Section 7.1.7.5

Result: 4.507 ms

☒ Pass ☐ Fail ☐ N/A

Comments:

EL_28 A device must transmit a chirp handshake no sooner than 2.5us and no later than 3ms when being reset from suspend or a full-speed state.

Reference documents: *USB 2.0 Specification*, Section 7.1.7.5

Result: 2.150511 ms☒ Pass ☐ Fail ☐ N/AComments:**C.5 Device Test J/K, SE0_NAK (EL_8, EL_9)**

EL_8 When either D+ or D- are driven high, the output voltage must be $400\text{mV} \pm 10\%$ when terminated with precision 45 Ohm resistors to ground.

Reference documents: *USB 2.0 Specification*, Section 7.1.1.3

Result:

Test	D+ Voltage	D- Voltage
J	-	12 mV
K	12 mV	-

☒ Pass ☐ Fail ☐ N/AComments:

EL_9 When either D+ or D- are not being driven, the output voltage must be $0\text{V} \pm 10\text{mV}$ when terminated with precision 45 Ohm resistors to ground.

Reference documents: *USB 2.0 Specification*, Section 7.1.1.3

Result:

	Voltage
D+	6 mV
D-	6 mV

☒ Pass ☐ Fail ☐ N/AComments:**C.6 Device Receiver Sensitivity (EL_16, EL_17, EL_18)**

EL_18 A high-speed capable device's Transmission Envelope Detector must be fast enough to allow the HS receiver to detect data transmission, achieve DLL lock, and detect the end of the SYNC field within 12 bit times.

Reference documents: *USB 2.0 Specification*, Section 7.1☒ Pass ☐ Fail ☐ N/AComments:

EL_17 A high-speed capable device must implement a transmission envelope detector that does not indicate squelch (i.e. reliably receive packets) when a receiver exceeds 150mV differential amplitude.

(*Note. A waiver may be granted if the receiver does not indicate Squelch at $\pm 50\text{mV}$ of 150mV differential amplitude.*)

This is to compensate for the oscilloscope probe point away from the receiver pin)

Reference documents: *USB 2.0 Specification*, Section 7.1

Results: 163.500 mV

☒ **Pass** ☐ Fail ☐ N/A

Comments: WAIVER

EL_16 A high-speed capable device must implement a transmission envelope detector that indicate squelch (i.e. never receive packets) when a receiver's input falls below 100mV differential amplitude.

(Note. A waiver may be granted if the receiver indicates Squelch at +/-50mV of 100mV differential amplitude. This is to compensate for the oscilloscope probe point away from the receiver pin)

Reference documents: *USB 2.0 Specification*, Section 7.1

Results: 149.200 mV

☒ **Pass** ☐ Fail ☐ N/A

Comments:

C.7 Bypass Capacitance Test

CRPB A USB device is required to expose a capacitance on the VBUS pin of its connector of CRPB. This capacitance shall be greater than CRPB min for voltages on the VBUS pin from 0V to 5.25V, regardless of whether the USB device is powered or unpowered

Reference documents: *USB 2.0 Specification*, Section 7.2.4

☒ **Pass** ☐ Fail ☐ N/A

Comments:

D. Testing References

D.1 Test Equipment

No	Vendor, Model	Version	Scope
1	Keysight, DSA91304A	SW: 05.60.00602 FW: 213	Electrical Tests
2	Keysight, 81134A	Ver 2.9.3	Electrical Tests
3	Keysight, U3402A	N/A	Electrical Tests
4	MQP, USB-PET	FW: 4.00	Check BC1.2 Implemented
5	Fluke, FLUKE 111	N/A	Current Measurement
6	DELL, XPS8700	BIOS: A08	Command Verifier Tests Interoperability Test

D.2 Test Tool

No	Vendor, Name	Version	Scope
1	Keysight, USB2.0 Compliance Test Software(N5416B)	03.93.0001	Electrical Tests
2	USB-IF, EHSETT	1.3.1.0	Electrical Tests
3	USB-IF, USB30CV	2.1.2.0	Command Verifier Test
4	USB-IF, USB20CV	1.5.2.0	Command Verifier Test
5	USB-IF, Interoperability Tool	12-18-15	Interoperability Tests
6	MQP, GraphicUSB	V4.68	Check BC1.2 Implemented

D.3 Reference

No	Name
1	Universal Serial Bus Revision 2.0 Specification(April 27, 2000) Including ENCs and errata
2	USB Implementers Forum Compliance Document USB 2.0 EHCI Interoperability Test Procedures Revision 1.0 (November 1, 2015)
3	USB Compliance Checklist Peripherals For the 2.0 USB Specification Checklist Version 1.09(January 16, 2012)

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